In the Claims

Claims 1-26 (Cancelled).

Please add new claims as follows:

27. (New) A static random access memory cell comprising:

first and second inverters respectively each including a first conductivity type of transistor having a respective gate, drain and source, the first and second inverters comprising a doped active area common to the drains of the first conductivity type transistors and comprising a contiguous region in the substrate extending from the drain of one of the first conductivity type transistors to the drain of the other first conductivity type transistor and a field oxide surrounding and isolating the contiguous region; and

an isolation gate formed on the common active area, between the drains of the first conductivity type transistors.

28. (New) The memory cell of claim 27, wherein the isolation gate comprises polysilicon.

29. (New) The memory cell of claim 27, wherein the first and second inverters include respective outputs, the memory cell further comprising:

a first access transistor having a first active terminal configured to be coupled to the output of the first inverter, a second active terminal configured to be coupled to a first bit line, and a gate configured to be coupled to a word line; and

a second access transistor having a first active terminal configured to be coupled to the output of the second inverter, a second active terminal configured to be coupled to a second bit line, and a gate configured to be coupled to the word line.

30. (New) The memory cell of claim 27, wherein:

the active area comprises a field oxide surrounding the contiguous region; and

the first and second inverters each comprise:

n-channel active areas each including a n-channel transistor; and

a field oxide surrounding and isolating each of the n-channel active areas.

31. (New) The memory cell of claim 27, wherein the first and second inverters comprise:

n-channel active areas each including a n-channel transistor; and

a field oxide surrounding and isolating each of the n-channel active areas.

32. (New) A static random access memory cell comprising:

a first p-channel pullup transistor having a gate, drain, and source;

a first n-channel pulldown transistor having a gate, drain, and source;

a second p-channel pullup transistor having a gate, drain, and source;

a second n-channel pulldown transistor having a gate, drain, and source; the source of the first pullup transistor being selectively coupled to a first voltage; the source of the second pullup transistor being selectively coupled to the first voltage; the drain of the first pulldown transistor being coupled to the drain of the first pullup transistor; the drains of the first and second pulldown transistors being formed in a common doped area surrounded and isolated by a dielectric region; the source of the first pulldown transistor being selectively coupled to a second voltage lower than the first voltage; the source of the second pulldown transistor being selectively coupled to the second voltage; the gate of the first pullup transistor being coupled to the gate of the first pulldown transistor; the gate of the second pullup transistor being coupled to the gate of the second pulldown transistor; the first pullup transistor and the first pulldown transistor together defining a first inverter having an output defined by the drain of the first pulldown transistor and an input defined by the gate of the first pulldown transistor, the second pullup transistor and the second pulldown transistor together defining a second inverter having an output defined by the drain of the second pulldown transistor and an input defined by the gate of the second pulldown transistor, the input of the first inverter

being coupled to the output of the second inverter, and the input of the second inverter being coupled to the output of the first inverter; and

a p-channel isolation transistor formed in the common area between the drains of the first and second pullup transistors.

33. (New) The memory cell of claim 32, wherein the source of the first p-channel transistor is coupled to the source of the second p-channel transistor, and to the gate of the p-channel isolation transistor.

34. (New) The memory cell of claim 32, wherein the p-channel isolation transistor comprises an active area that is common to both the first pullup transistor and the second pullup transistor.

35. (New) The memory cell of claim 32, wherein the source of the first pullup transistor is coupled to the first voltage, wherein the source of the second pullup transistor is coupled to the first voltage, wherein the source of the first pulldown transistor is coupled to the second voltage, wherein the gate of the p-channel isolation transistor is coupled to the first voltage, and wherein the source of the second pulldown transistor is coupled to the second voltage.

36. (New) The memory cell of claim 32, wherein the p-channel isolation transistor comprises an active area that is common to both the drain of the first pullup transistor and the drain of the second pullup transistor.

37. (New) The memory cell of claim 32, further comprising a first bit line; a second bit line; a word line; a first access transistor having a first active terminal coupled to the output of the first inverter, having a second active terminal coupled to the first bit line, and having a gate adapted to be coupled to the word line; and a second access transistor having a first active terminal coupled to the output of the second inverter, having a second active terminal coupled to the second bit line, and having a gate coupled to the word line.